Abstract

A switch/router circuit integrates a multi-port memory array with the Media Access Control (MAC) units to facilitate direct transfer of packet payloads to the destination port. The store and forward functions are performed using a single memory cell with multiple pass gates, one pass gate designated for each MAC port. That is, a switch router is implemented using the multi-port memory array such that the number of ports in each memory cell is proportional to the number of MACs integrated in the single monolithic chip. An arbitrator arbitrates between the integrated ports, a lookup table identifies the destination port and a system controller controls all of the integrated elements.